JP-10-290012

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the active matrix liquid crystal display using TFT as a switching element and its manufacture method of dual gate structure about active matrix liquid crystal display and its manufacture method.
[0002]
[Description of the Prior Art] As for the TFT of dual gate structure, some things are already proposed for the purpose of improvement in transistor characteristics. For example, drawing 6 - drawing 12 are the active matrix liquid crystal display (henceforth the 1st conventional example) which made the switching element TFT of the dual gate structure indicated by JP,2-304532,A, and show this in order of a manufacturing process. in addition, the cross section which meets an A-A'B-B [in / (a) / in the cross section which meets a line, and (c)]' line / in / (a) / on each drawing and / (a) and / in (b)] -- it comes out / a plan

[0003] the photo lithography [films / transparent electric conduction / 106 /, such as an indium-stannic-acid-ized film (it is hereafter described as ITO) which formed membranes by sputtering on the transparent insulating substrate 101 which drawing 6 shows the 1st process and consists of glass etc.,] process using the photoresist 107, and an ITO sentiment -- therefore, patterning is dirtily carried out to the configuration of the pixel electrode 8
[0004] the photo lithography [metal membranes / 102 /, such as chromium (it is hereafter described as Cr) which formed membranes by sputtering on the substrate which drawing 7 shows the 2nd process and the 1st process ended,] process using the photoresist 107, and Cr sentiment -- therefore, patterning is dirtily carried out to the configuration of the gate bus line 2 connected with the bottom gate electrode 1 at this, and the contact section 10
[0005] Drawing 8 on the substrate which shows the 3rd process and the 2nd process ended The silicon nitride which formed membranes by the plasma CVD (Chemical Vapor Deposition) method (It is hereafter described as SiN) etc. -- an insulator layer 103 -- amorphous silicon (It is hereafter described as a-Si) etc. -- the semiconductor film 104 -- n type amorphous silicon (It is hereafter described as n+a-Si) etc. -- the photo lithography [' / n-type-semiconductor film 104] process using the photoresist 107, and n+a-Si/a-Si dry cleaning -- therefore, patterning is dirtily carried out to the configuration of an island 6
[0006] the photo lithography process and SiN dry cleaning which used the photoresist 107 on the substrate which drawing 9 shows the 4th process and the 3rd process ended -- therefore, a contact hole 7 is formed dirtily
[0007] the photo lithography [' / metal membrane 102/, such as Cr which formed membranes by sputtering on the substrate which drawing 10 shows the 5th process and the 4th process ended,] process using the photoresist 107, and Cr sentiment -- therefore, patterning is dirtily carried out to the configuration of the drain bus line 4 connected with the drain electrode 3 at this, and the source electrode 5
[0008] n+a-Si between the drain electrode 3 of the substrate which drawing 11 shows the 6th process and the 5th process ended, and the source electrode 5 -- n+a-Si dry cleaning -- the photo lithography process and SiN dry cleaning using the photoresist 107 after removing more dirtily (the following and a channel -- it is said that it is dirty) and forming the insulator layers 105, such as SiN, by plasma CVD -- therefore, contact hole 7' is formed dirtily
[0009] the photo lithography [" / metal membrane 102/, such as Cr which formed membranes by sputtering on the substrate which drawing 12 shows the 7th process and the 6th process ended,] process using the photoresist 107, and Cr sentiment -- therefore, patterning is dirtily carried out to the configuration of the top gate electrode 9
[0010] If the above is summarized, in order to manufacture the TFT of the 1st conventional example ** The patterning process of the pixel electrode 8, ** bottom gate electrode 1, the gate bus line 2, the patterning process of the contact section 10, ** The patterning process of an island 6, the formation process of the ** contact hole 7, ** The patterning process of the drain electrode 3, the drain bus line 4, and the source electrode 5, the formation process of ** contact hole 7', and no less than 7 times of the photo lithography processes of patterning process ** of ** top gate electrode 9 are needed. Thus, if there is much number of times of a photo lithography process, not only the cost rise by equipment use man days, such as the amount of the indirect members used, such as a photo mask, and an aligner, but the fall of the yield etc. will take place, and the trouble that a manufacturing cost rises sharply will arise.
[0011] Moreover, since the gate bus line 2 and the pixel electrode 8 are formed as a trouble resulting from structure, without minding an insulator layer, the pixel electrode 8 will not be able to be made to overlap the gate bus line 2, but a limit will be given

to high numerical aperture-ization.
[0012] Then, as the method of compensating the fault of the 1st conventional example, it is the fewer number of photo lithography processes, and layer separation of a pixel electrode, a gate bus line, and the drain bus line is carried out by the insulator layer, and the manufacture method (henceforth the 2nd conventional example) which produces the TFT of dual gate structure is indicated by JP,5-53147,A.
[0013] Drawing 13 - drawing 17 show the active matrix liquid crystal display of the 2nd conventional example in order of a manufacturing process. in addition, the cross section which meets an A-A'B-B [in / (a) / in the cross section which meets a line, and (c)]' line / in / (a) / on each drawing and / (a) and / in (b)] -- it comes out / a plan
[0014] the photo lithography [metal membranes / 102 /, such as Cr which formed membranes by sputtering on the transparent insulating substrate 101 which drawing 13 shows the 1st process and consists of glass etc.,] process using the photoresist 107, and Cr sentiment -- therefore, patterning is dirtily carried out to the configuration of the gate bus line 2 connected with the bottom gate electrode 1 at this
[0015] the photo lithography [' / n-type-semiconductor film 104/, such as the semiconductor films 104, such as the insulator layers 103, such as SiN which formed membranes by the plasma CVD method on the substrate which drawing 14 shows the 2nd process and the 1st process ended, and a-Si, and n+a-Si] process using the photoresist 107, and n+a-Si/a-Si dry cleaning -- therefore, patterning is dirtily carried out to the configuration of an island 6
[0016] the photo lithography [' / metal membrane 102/, such as Cr which formed membranes by sputtering on the substrate which drawing 15 shows the 3rd process and the 2nd process ended,] process using the photoresist 107, and Cr sentiment -- therefore, patterning is dirtily carried out to the configuration of the drain electrode 3, the drain bus line 4 connected to this, and the source electrode 5
[0017] the photo lithography process and SiN dry cleaning using the photoresist 107 after drawing 16's showing the 4th process, giving CHANERUETCHI to the substrate which the 3rd process ended and forming the insulator layers 105, such as SiN, by plasma CVD -- therefore, opening of a contact hole 7 and the planned pixel electrode formation site is formed dirtily
[0018] the photo lithography [films / transparent electric conduction / 106 /, such as ITO which formed membranes by sputtering on the substrate which drawing 17 shows the 5th process and the 4th process ended,] process using the photoresist 107, and an ITO sentiment -- therefore, patterning is dirtily carried out to the configuration of the pixel electrode 8 and the top gate electrode 9

[0019]
[Problem(s) to be Solved by the Invention] However, there were the respectively following troubles in the above-mentioned conventional example. As for the 1st trouble, in the case of the 1st conventional example (JP,2-304532,A), cost becomes high. The reason is that the patterning process of ** pixel electrode, ** bottom gate electrode, a gate bus line, the patterning process of the contact section, the patterning process of ** island, the formation process of ** contact hole, ** drain electrode, a drain bus line, the patterning process of a source electrode, the formation process of ** contact hole, and 7 times of the photo lithography processes of patterning process ** of ** top gate electrode are needed, in order to manufacture the TFT of the 1st conventional example. And when there is much number of times of a photo lithography process in this way, it is for not only the cost rise by equipment use man days, such as the amount of the indirect members used, such as a photo mask, and an aligner, but the fall of the yield etc. to take place, and for a manufacturing cost to rise sharply.
[0020] In the case of the 1st conventional example, the 2nd trouble is receiving a limit in high numerical aperture-ization as a liquid crystal display. The reason is since the gate bus line and the pixel electrode are formed without minding an insulator layer, not made to the structure of making a pixel electrode overlapping a gate bus line.
[0021] In the case of the 2nd conventional example, I hear that the stage piece of a top gate electrode tends to occur, and there is the 3rd trouble. the reason -- the 2nd conventional example -- reverse stagger structure -- it is -- a channel -- it is necessary to thicken the semiconductor film used as an island to thousands ofA for a dirty variation margin Therefore, since a top gate electrode serves as structure with a big level difference with the level difference of an island, the stage piece of a top gate electrode becomes easy to happen. In addition, the processability with wet ITO depended dirtily is bad, and it is difficult to make it thickness 1000A or more.
[0022] In the case of the 2nd conventional example, I hear that a transistor performance tends to be influenced of light, and the 4th trouble has it. Since the 2nd conventional example is using the transparent electric conduction film for a top gate electrode, the reason has the structure where the upper part of a transistor is not shaded. Therefore, it is because the leakage current at the time of transistor-off becomes large by the light from the transistor upper part.
[0023] In the case of the 2nd conventional example, I hear that it is easy to generate an open circuit of a drain bus line, and there is the 5th trouble. The reason is that the formation process of a drain bus line is after an island formation process, i.e., a plasma CVD process with many particle yields, in the 2nd conventional example. Therefore, it becomes easy to generate an open circuit of a drain bus line especially by the particle which adhered into the plasma CVD process.
[0024] this invention is made in order to solve the above-mentioned technical problem, and it aims at aiming at improvement in the yield and a performance by improving the structure of TFT in the active matrix liquid crystal display which made TFT of dual gate structure the switching element, and its manufacture method, without making the number of photo lithography processes increase.
[0025]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the active matrix liquid crystal display of this

invention The gate bus line connected to the bottom gate electrode and this which were formed on the insulating substrate, These bottom gate electrode and a gate bus line The 1st insulator layer of a wrap, The drain bus line and source electrode which were connected to the drain electrode and this which were formed on the 1st insulator layer, The island formed by the semiconductor film and the 2nd insulator layer from the lower layer side so that it might lap with a part of drain electrode and source electrode at least], The top gate electrode and pixel electrode which consist an island of a transparent electric conduction film formed on the 3rd insulator layer of a wrap, and the 3rd insulator layer, While coming to **** and connecting a bottom gate electrode and a top gate electrode electrically through a contact hole, it is characterized by connecting a source electrode and a pixel electrode electrically through a contact hole.

[0026] Moreover, the manufacture method of the active matrix liquid crystal display of this invention After forming an electric conduction film on an insulating substrate, by carrying out patterning of this electric conduction film The process which forms the gate bus line connected to a bottom gate electrode and this, After forming an electric conduction film on the process which forms the 1st insulator layer of a wrap for these bottom gate electrode and a gate bus line, and the 1st insulator layer, by carrying out patterning of this electric conduction film The process which forms the drain bus line and source electrode which were connected to a drain electrode and this, After forming a semiconductor film and the 2nd insulator layer one by one on a drain electrode and a source electrode, by carrying out patterning of these semiconductor film and the 2nd insulator layer By carrying out patterning of the 3rd insulator layer and the insulator layer under it to the process which forms the island which laps with a part of drain electrode and source electrode [at least], and the process which forms the 3rd insulator layer of a wrap for an island The process which forms simultaneously the contact hole for a bottom gate electrode-top gate electrode flow, and the contact hole for a source electrode-pixel electrode flow, After forming a transparent electric conduction film on the 3rd insulator layer, it is characterized by having the process which forms the pixel electrode electrically connected with the top gate electrode and source electrode which were electrically connected with the bottom gate electrode by carrying out patterning of this transparent electric conduction film. And in the above-mentioned manufacture method, in case membrane formation of the aforementioned semiconductor film and the 2nd insulator layer is performed, phosphine plasma treatment and a plasma CVD method can be used.

[0027] In order to realize a high numerical aperture and manufacture process shortening, it is effective as basic structure of a liquid crystal display to form a pixel electrode in the best layer. Furthermore, for increase of the ON state current of a transistor, and reduction of the OFF state current, it is effective to make it dual gate structure. Therefore, TFT is formed with the yield sufficient [how] using transparent electric conduction films, such as the thin ITO same to a top gate electrode as a pixel electrode, and it becomes the technical point whether a property is secured. Then, it describes below how this purpose can be attained with the composition of this invention.

[0028] Since the TFT in this invention is order stagger structure fundamentally, it can make thin thickness of the semiconductor film used as an island to hundreds ofA. For this reason, an open circuit of the top gate resulting from the level difference of an island can be prevented, and the yield can be improved.

[0029] By the way, usually, when light is irradiated by the semiconductor film, a hole and an electron occur and it becomes the cause of the leakage current at the time of transistor-off. However, when the thickness of a semiconductor film becomes thin, the distance of a front channel and a back channel approaches, and since the hole and electron which are generated by light recombine with the defect of the back channel section, it disappears. Therefore, increase of the leakage current at the time of the transistor-off by light can be prevented, and even if there is no shading film on a transistor, it becomes possible to maintain normal transistor characteristics. Furthermore, since it is dual gate structure, reduction of the leakage current by reversing the whole semiconductor film is also expectable.

[0030] Moreover, by the manufacture method of this invention, the gate bus line and the drain bus line are formed before a plasma CVD process with many particle yields. Therefore, a bus-line open circuit of a particle reason at a plasma CVD process is lost, and a bus-line burnout rate decreases sharply. Consequently, the effect that the yield improves is also acquired.

[0031]

[Embodiments of the Invention] Hereafter, the form of 1 operation of this invention is explained with reference to drawing 1 - drawing 5 . Drawing 1 - drawing 5 show a part of active-matrix plated circuit (active matrix liquid crystal display) which made the switching element TFT of the dual gate structure which is the form of this operation in order of a manufacturing process. in addition, the cross section which meets an A-A'B-B [in / (a) / in the cross section which meets a line, and (c)]' line / in / (a) / on each drawing and / (a) and / in (b)] -- it comes out / a plan

[0032] the photo lithography process and Cr sentiment using the photoresist 107 after forming the metal membrane 102 (electric conduction film) of 1500A of thickness which consists of Cr etc. by sputtering on the transparent insulating substrate 101 which drawing 1 shows the 1st process and consists of a glass substrate etc. -- patterning is carried out more dirtily and the gate bus line 2 connected with the bottom gate electrode 1 at this is formed

[0033] Drawing 2 on the substrate which shows the 2nd process and the 1st process ended After forming the insulator layer 103 (the 1st insulator layer) of 3000A of thickness which consists of a silicon oxide etc. by ordinary-pressure CVD, Metal membrane of 1500A of thickness which consists of Cr etc. by sputtering 102' (electric conduction film) is formed. the photo lithography process and Cr sentiment using the photoresist 107 -- patterning is carried out more dirtily and the drain bus line 4 and the source electrode 5 which were connected with the drain electrode 3 at this are formed

[0034] a photo lithography process and SiN/a-Si dry cleaning drawing 3 shows the 3rd process, forms the insulator layer 105 (the 2nd insulator layer) of 500A of thickness which consists of a semiconductor film 104 of 500A of thickness which consists of a-Si etc. by phosphine (PH3) plasma treatment and the plasma CVD method on the substrate which the 2nd process ended, SiN, etc.,

and using the photoresist 107 -- patterning is carried out more dirtily and an island 6 is formed

[0035] Drawing 4 on the substrate which shows the 4th process and the 3rd process ended After forming insulator layer of 2500A of thickness which consists of SiN etc. by plasma CVD method 105' (the 3rd insulator layer), Therefore, patterning is carried out dirtily. the photo lithography process and SiN dry cleaning using the photoresist 107 -- The contact holes 7 and 7 for making it flow through the bottom gate electrode 1, the top gate electrode and the source electrode 5 which are formed at the following process, and the pixel electrode formed at the following process, respectively are formed.

[0036] Drawing 5 on the substrate which shows the 5th process and the 4th process ended After forming the transparent electric conduction film 106 of 500A of thickness, such as ITO, by sputtering, Therefore, patterning is carried out dirtily. the photo lithography process and ITO sentiment using the photoresist 107 -- The pixel electrode 8 electrically connected with the source electrode 5 through the contact hole 7 and the top gate electrode 9 electrically connected with the bottom gate electrode 1 through the contact hole 7 are formed.

[0037] Thus, according to the form of this operation, it becomes possible to manufacture TFT at 5 times of the photo lithography processes of patterning process ** of the patterning process of the patterning process of ** bottom gate electrode 1 and the gate bus line 2, ** drain electrode 3, the drain bus line 4, and the source electrode 5, the patterning process of the ** island 6, the formation process of the ** contact hole 7, ** pixel electrode 8, and the top gate electrode 9. Therefore, compared with the case of the conventional example 1, the number of times of a photo lithography process can become fewer, and a manufacturing cost can be reduced as a result of reduction of equipment use man days, such as the amount of the indirect members used, such as a photo mask, and an aligner, improvement in the yield, etc.

[0038] Moreover, since the gate bus line 2 and the pixel electrode 8 are formed through the insulator layer 103 unlike the structure of the conventional example 1, the structure of the TFT of the form of this operation can make the pixel electrode 8 able to overlap the gate bus line 2, and can attain high numerical aperture-ization.

[0039] And since it is order stagger structure and the semiconductor film 104 used as an island 6 can be made thin to hundreds ofA (the form of this operation 500A), the level difference of the top gate electrode 9 becomes smaller than before, and the probability that the stage piece of the top gate electrode 9 will be generated decreases. Moreover, since the gate bus line 2 and the drain bus line 4 are formed before a plasma CVD process with many particle yields, generating of the bus-line open circuit resulting from this particle is also suppressed. Consequently, improvement in the yield can be aimed at. When the liquid crystal panel of 400 sheets was actually made as an experiment using the manufacture method of the form this operation, there is no generating of the stage piece of a top gate electrode, open circuits of a gate bus line and a drain bus line are two panels and four panels, respectively, and it was checked that it has fully decreased compared with 2 - 4% of conventional poor incidence rate.

[0040] Furthermore, with the structure of the form of this operation, since the top gate electrode 9 is also formed by the transparent electric conduction films 106, such as the same ITO as the pixel electrode 8, although a transistor is not shaded, the leakage current at the time of transistor-off is stopped by operation of having made the semiconductor film 104 of an island 6 thin, and the stable transistor performance which cannot be easily influenced of light can be demonstrated by it.

[0041] in addition, the technical range of this invention can add various change in the range which is not limited to the form of the above-mentioned implementation and does not deviate from the meaning of this invention For example, what [not only] was shown with the form of this operation about the kind of each film used for TFT, thickness, the manufacture conditions of each process, etc. but the thing adopted suitably is possible.

[0042]

[Effect of the Invention] As mentioned above, according to this invention, the following effects are acquired as explained in detail. The 1st effect can reduce an open circuit of a top gate electrode, and its yield improves. The reason is because thickness of the semiconductor film used as an island can be made thin to about hundreds ofA by considering as order stagger structure.

[0043] The 2nd effect is being able to reduce the influence on the transistor performance by light. It is because this reason can also make thinly thickness of the semiconductor film which serves as an island by considering as order stagger structure be the same as that of the case of the 1st effect to about hundreds ofA. Usually, when light is irradiated by the semiconductor film, a hole and an electron occur and it becomes the cause of the leakage current at the time of transistor-off. However, when the thickness of a semiconductor film becomes thin, the distance of a front channel and a back channel approaches, and since the hole and electron which are generated by light recombine with the defect of the back channel section, it disappears. Therefore, increase of the leakage current at the time of the transistor-off by light can be prevented.

[0044] The 3rd effect can reduce a gate bus line and a drain bus-line burnout rate, and its yield improves. The reason forms the gate bus line and the drain bus line before a plasma CVD process with many particle yields. Therefore, it is because the bus-line open circuit resulting from the particle in a plasma CVD process is lost.

[0045] These effects can be done so in this invention, consequently improvement in the yield in active matrix liquid crystal display, improvement in a property, and reduction of a manufacturing cost can be realized.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] the manufacture method of the active matrix liquid crystal display of the gestalt 1 operation of this invention -- setting -- (a) -- the plan showing the state at the time of the 1st process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 2] **** (a) -- the plan showing the state at the time of the 2nd process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 3] **** (a) -- the plan showing the state at the time of the 3rd process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 4] **** (a) -- the plan showing the state at the time of the 4th process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 5] **** (a) -- the plan showing the state at the time of the 5th process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 6] the manufacture method of the active matrix liquid crystal display of the 1st conventional example -- setting -- (a) -- the plan showing the state at the time of the 1st process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 7] **** (a) -- the plan showing the state at the time of the 2nd process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 8] **** (a) -- the plan showing the state at the time of the 3rd process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 9] **** (a) -- the plan showing the state at the time of the 4th process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 10] **** (a) -- the plan showing the state at the time of the 5th process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 11] **** (a) -- the plan showing the state at the time of the 6th process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 12] **** (a) -- the plan showing the state at the time of the 7th process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 13] the manufacture method of the active matrix liquid crystal display of the 2nd conventional example -- setting -- (a) -- the plan showing the state at the time of the 1st process, and the cross section which meets the A-A'B-B of cross section which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 14] **** (a) -- the plan showing the state at the time of the 2nd process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 15] **** (a) -- the plan showing the state at the time of the 3rd process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 16] **** (a) -- the plan showing the state at the time of the 4th process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Drawing 17] **** (a) -- the plan showing the state at the time of the 5th process, and the cross section which meets the A-A'B-B of cross section [which meets a line], (c), and (a)' line of (b) and (a) -- it comes out
[Description of Notations]
1 Bottom Gate Electrode
2 Gate Bus Line
3 Drain Electrode
4 Drain Bus Line
5 Source Electrode
6 Island
7 7' Contact hole
8 Pixel Electrode
9 Top Gate Electrode

10 Contact Section
101 Insulating Substrate
102 Metal Membrane (Object for Bottom Gates, Electric Conduction Film)
102' metal membrane (the object for source drains, electric conduction film)
102" metal membrane (the object for the top gates, electric conduction film)
103 Insulator Layer (Bottom Gate Insulator Layer, 1st Insulator Layer)
104 Semiconductor Film
104' n-type-semiconductor film
105 Insulator Layer (1St Top Gate Insulator Layer, 2nd Insulator Layer)
105' insulator layer (2nd top gate insulator layer, the 3rd insulator layer)
106 Transparent Electric Conduction Film
107 Photoresist

[Translation done.]